# XC61F Series Voltage Detectors with Built-in Delay Circuits

## Application Notes

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## ❍ Introduction

The XC61F series are highly accurate, low power consumption voltage detectors with built-in delay circuits, manufactured using laser trimming and CMOS process technologies.

Detect voltage is extremely accurate with minimal temperature drift. Both CMOS and N-channel open drain output configurations are available.

Since the delay circuits are built-in, there is no need for peripherals and therefore high density mounting is possible.

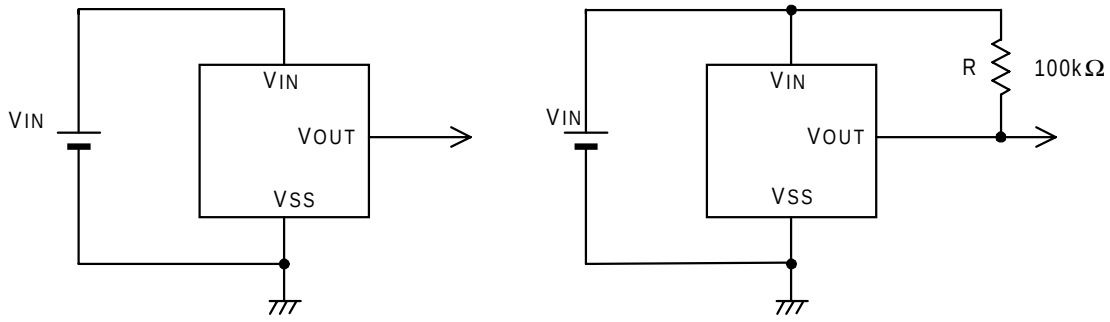
## ❍ Advantages of a Delay Circuit

In general, voltage detectors detect fall voltages and release rise voltages. Once power has been switched on and the internal circuitry of the CPU and other logic systems has been stabilized, reset will be released.

Although the connection of an external capacitor and resistor to either the input or output side is regarded as the conventional method for obtaining delay time, peripheral variance and/or power supply rise times lead to problems because of the large fluctuations in delay time that such variances cause.

With the XC61F series, a circuit that generates delay time at power-up is built into the IC so that systems can be stabilized without the worries of peripheral variance. Therefore, the XC61F can be used for reset circuits without having to use peripherals.

## ❍ Standard Circuits




XC61FC series　　XC61FN series

## ❍ Notes on Use

**1. Oscillation as a result of output current with CMOS output configurations**

As oscillation may occur due to load current (IOUT) with CMOS output configurations if a resistor is present between the VIN pin and the power supply, we recommend that you use Nch open drain output configurations where RIN is used.

**N.B.**

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow through RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin.

When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.

Oscillation may occur with this " release – detect – release" repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

Note : Do not use RIN with CMOS output configurations as oscillation may occur.

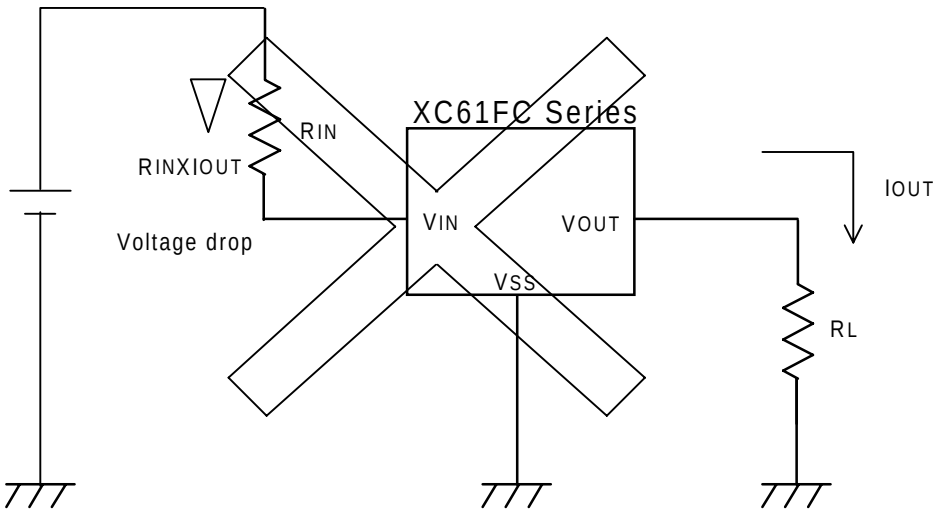



Diagram 1. Oscillation resulting from output current

**2. Oscillation as a result of through current**

Please note that if a resistor is connected between the VIN pin and the power supply with CMOS output configurations (irrespective of N-channel output configurations), oscillation may occur as a result of through current at the time of voltage release.
(Please refer to Diagram 2)
Through current is the current that flows excessively when the IC's internal circuit voltage level changes (during release and detect operations).

**N.B.**

When the voltage applied at IN rises, release operations commence, the detector's output voltage increases and through current flows. Because a voltage drop (RIN x ISS) is produced at the RIN resistor, located between the input (IN) and the VIN pin, this through current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin.
When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, through current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.
Oscillation may occur with this " release – detect – release" repetition.
However, since hysteresis exists during detect operations, oscillation is unlikely to occur. In comparison to N-channel output configurations, through current in the final stages is larger with CMOS output configurations, which tends to result in oscillation occurring somewhat more easily.

Note : Do not use RIN with CMOS output configurations as oscillation may occur.

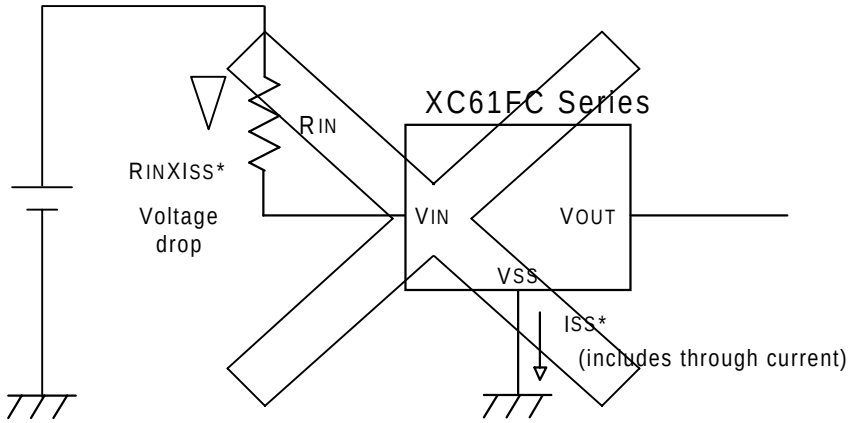
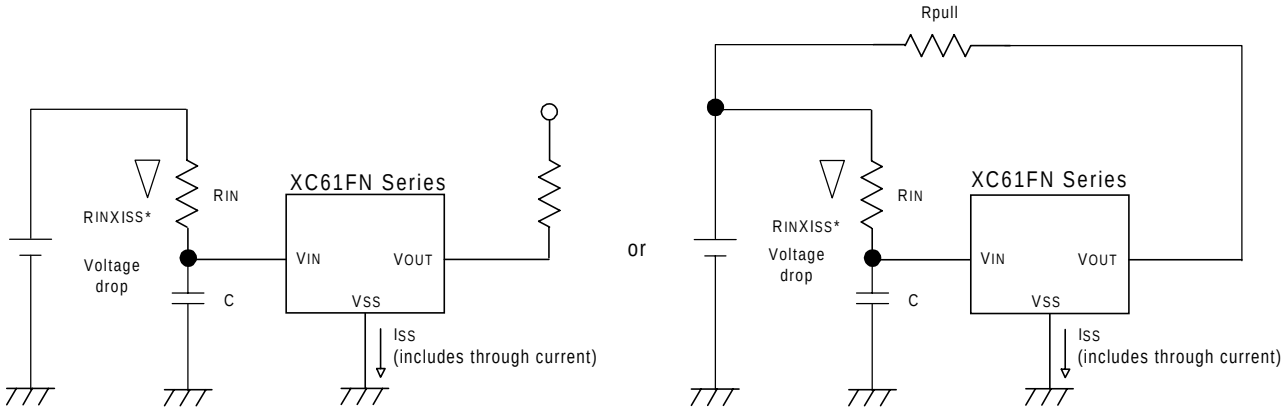



Diagram 2. Oscillation resulting from through current

Always use the N-channel open drain output configuration if an input resistor (RIN) is to be used and/or the input voltage is to be divided. (Please refer to Diagram 3 )
With an input resistor (RIN) present, release voltage will rise if a pull up resistor (Rpull) is connected between the VIN – VOUT pins and input voltage is divided between RIN and Rpull. It is therefore recommended that the pull up resistor be connected to the power supply side. (Please refer to Application Circuit 2, page 8)




* Pull up resistor connected to separate power supply

* Pull up resistor connected to input

Diagram 3. Example circuit with Input Resistor connected

N.B. Please ensure that RIN = less than 10kΩ, C = more than 0.1μF

Please be aware that both detect and release voltages will rise due to voltage drops at RIN brought about by the IC's supply current.

**N.B.**

In general, voltage detectors are highly susceptible to oscillation due to input impedance, but because a delay exists at time of release with the XC61F series, oscillation due to input impedance is unlikely. However, we still suggest that input impedance is kept as low as possible.

## 3. Operational errors resulting from steep frequency inputs

Should steep start up voltages be input at the VIN pin, frequencies output from VOUT may become distorted so please regulate input frequency start up time (MIN) to a standard of more than several μ seconds/V.

## 4. Power Dissipation Pd

Please observe the following points :

CMOS

$(V_{IN} - V_{OUT}) \times I_{OUT} < Pd$ : Release time (PchFET : ON)

$V_{OUT} \times I_{OUT} < Pd$ : Detect time (NchFET : ON)

Should output ($V_{OUT}$) short to ground during release operations, the resulting heat from the loss at $V_{IN} \times I_{OUT}$ may cause damage to the IC so please take all necessary precautions.

N-channel open drain

$V_{OUT} \times I_{OUT} < Pd$ : Detect time

**5. Pull up resistor with N-channel open drain configurations**

If the pull up resistance value is extremely large, output voltage may drop during release operations as a result of the N-channel transistor leak current within the IC.
It is therefore recommended that a pull up resistance of less than 470kΩ be used.
(a pull up resistor is not necessary with CMOS output configurations)

## ❍ Application Circuits

### 1. High voltage detection circuit

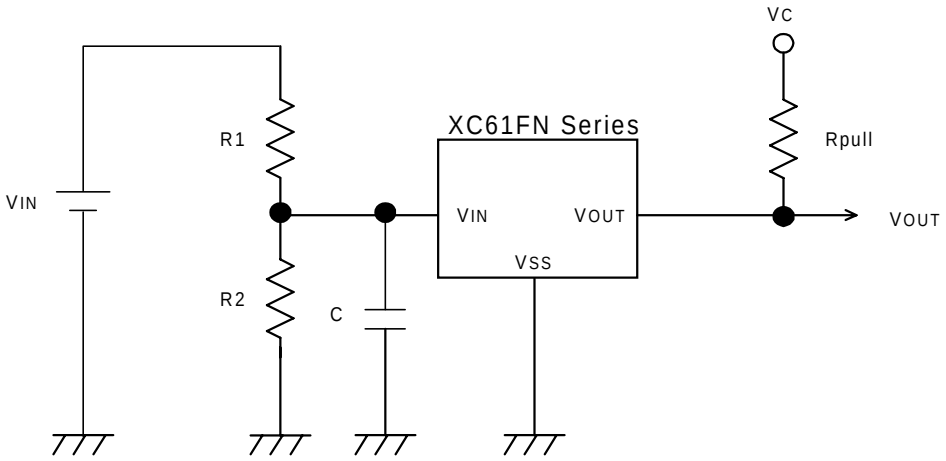



Diagram. High voltage detection circuit

XC61FN series

Peripherals :

R1 : 10kΩ

R2 : 5kΩ

Ex.) Detect voltage $V_{DF}$ = 3.0V

Set-up detect voltage $V_{DH}$ = 9.0V

Hysteresis range increases from 0.15V(typ) to 0.45V

(Please refer to the notes on detect voltage $V_{DH}$ and hysteresis range $V_{HYSH}$ provided below)

C : 0.1μF

Rpull : 100kΩ

Notes on Use :

It is recommended that R1 = less than 10kΩ and that C = more than 0.1μF in order to avoid oscillation.

Note that the above does not apply to CMOS output (XC61FC series) configurations.

Notes :

The value for detect voltage $V_{DH}$ and hysteresis range $V_{HYSH}$ can be calculated as follows :

$V_{DH} = V_{DF} \cdot (R_1 + R_2) \div R_2$ (V)

$V_{HYSH} = V_{HYS} \cdot (R_1 + R_2) \div R_2$ (V)

where $V_{DF}$ = the IC's detect voltage value

$V_{DH}$ = the actual circuit's detect voltage value

$V_{HYS}$ = the IC's hysteresis range

$V_{HYSH}$ = the actual circuit's hysteresis range

Please note that due to the IC's supply current $I_{SS}$, $V_{DH}$ will be higher than, and $V_{HYSH}$ will be larger than, the calculated values.

Explanation :

Should the required voltage detector be unavailable, it is possible to achieve a detect voltage higher than the IC's established value by using divided resistors, but only with N- channel open drain output configurations.

**2. Hysteresis range enlargement circuit**

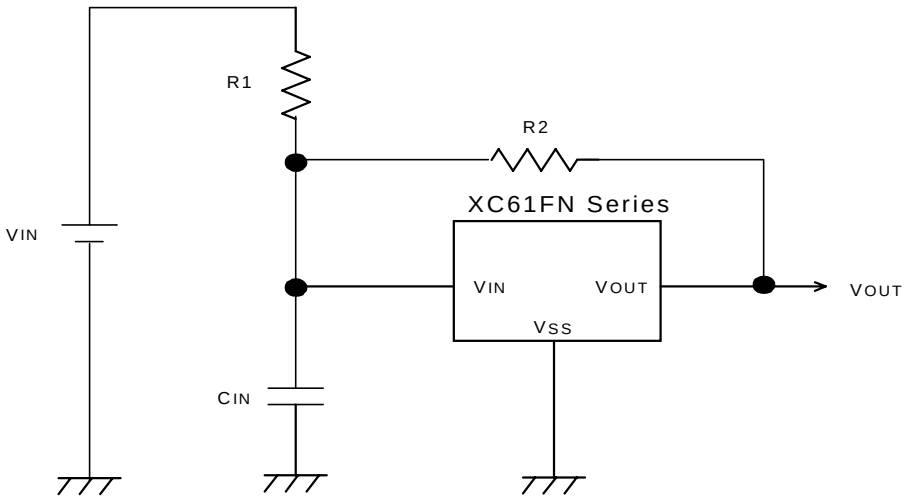



Diagram. Hysteresis range enlargement

XC61FN series

Peripherals :

$R_1$ : 3kΩ

$R_2$ : 33kΩ

$C_{IN}$ : 0.1μF

Ex.) Release voltage $V_{DR}$ = 3.15V, $R_1$=3kΩ, $R_2$=33kΩ

Set-up release voltage $V_{DR1}$ = 3.44V

Release voltage therefore increases by 0.29V

Please refer to the notes on release voltage provided

Notes on Use :

It is recommended that $R_1$ = less than 10kΩ and that $C_{IN}$ = more than 0.1μF in order to avoid oscillation.

Note that the above does not apply to CMOS output (XC61FC series) configurations.

Notes :

The value for release voltage $V_{DR1}$ can be calculated as follows :

$$V_{DR1} = V_{DR} \cdot (R_1 + R_2) \div R_2$$

where $V_{DR}$ = the IC's release voltage value

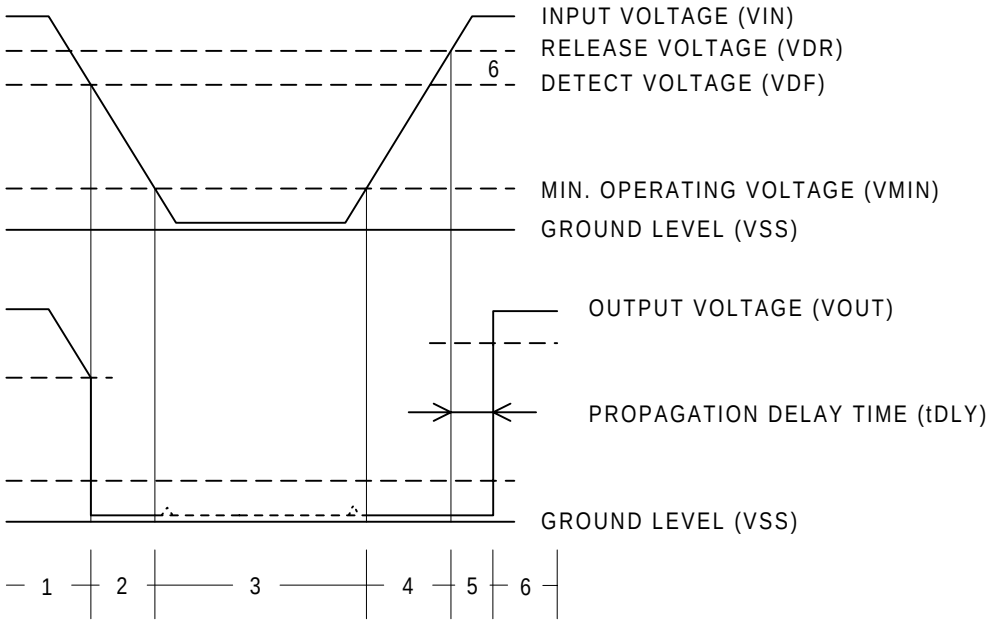
$V_{DR1}$ = the actual circuit's release voltage value

Explanation :

With N- channel open drain output configurations it is possible to enlarge the hysteresis range without having to change detect voltage.

## ❍ Appendix

### A1. XC61F Series Operational Explanation




**Functional Explanation**

1. Should a voltage higher than the release voltage ($V_{DR}$) be applied at the power supply pin ($V_{IN}$), voltage will gradually decrease.
   Should a voltage higher than the detect voltage ($V_{DF}$) be applied at the power supply pin ($V_{IN}$), a voltage equal to the input pin voltage level will be output at the output pin ($V_{OUT}$)
   Note that as a condition of high impedance exists at the $V_{OUT}$ pin with Nch open drain configurations, the voltage will be pull up voltage should the pin be pulled up.
2. When $V_{IN}$ falls below $V_{DF}$, $V_{OUT}$ will equal ground voltage ($V_{SS}$).
   (Also applicable to Nch open drain configurations)
3. When $V_{IN}$ falls to a level below that of the minimum operating voltage ($V_{MIN}$), output becomes unstable.
   Note that as the output pin is generally pulled up with N-channel open drain output configurations, output will be equal to pull up voltage.
4. When $V_{IN}$ rises above the $V_{SS}$ level (excluding the area lower than min. operating voltage), output voltage ($V_{OUT}$) will remain equal to $V_{SS}$ until the release voltage level ($V_{DR}$) is reached.
5. Although input voltage ($V_{IN}$) will exceed detect release voltage ($V_{DR}$) as it

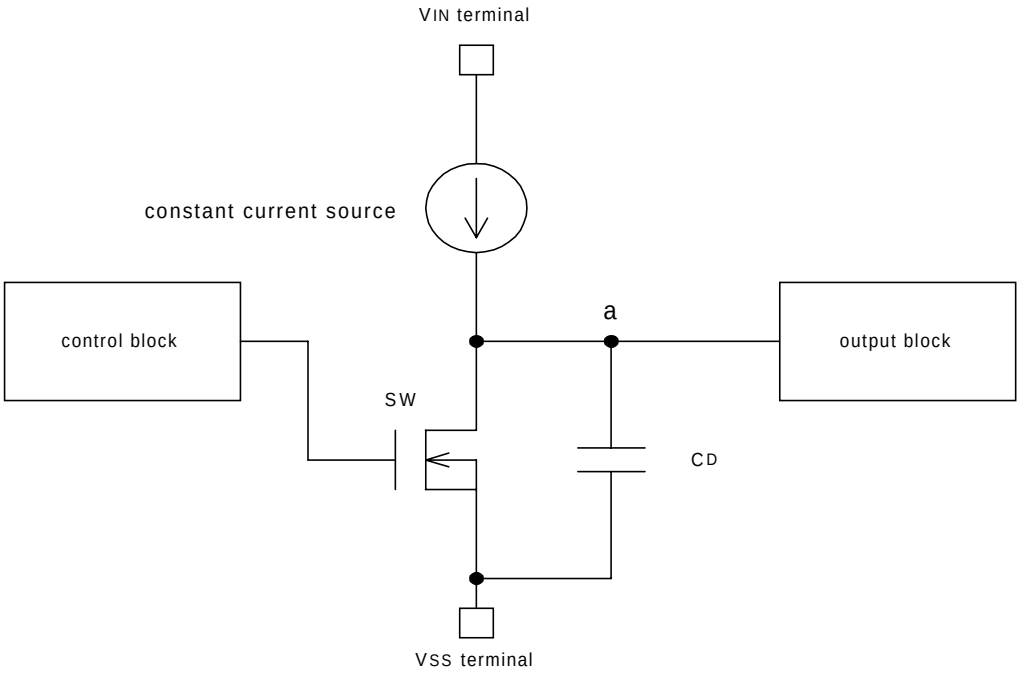
rises, output voltage (VOUT) maintains the ground voltage level as a result of the delay circuit.

6. Once propagation delay time has passed, input pin voltage (VIN) will be output at the output pin (VOUT).
   Note that as a condition of high impedance exists with Nch open drain configurations, the voltage will be pull up voltage

NOTE :

(1) The difference between VDR and VDF represents the hysteresis range.
(2) Propagation delay time (tDLY) is the time that it takes for input voltage (VIN) to be output at the output pin (VOUT) once the input voltage (VIN)has exceeded detect release voltage (VDR)

## A2. Delay Operations




Release Operations :

1. Input voltage (VIN) rises and the IC's operations commence :
   SW : ON
   The voltage at 'a' will be equal to the ground voltage (VSS) level.
2. Input voltage rises further, exceeding release voltage :
   SW : OFF (via the control block signal)
   Constant current source charges condenser CD and the voltage at 'a' rises above the ground voltage (VSS) level.

3. The voltage at ‘a’ exceeds the threshold voltage value (*) :
   Release operation’s signal sent to output block.

Detect Operations :

4. VIN drops from being above release voltage level to being below detect voltage level :
   SW : ON
   The voltage at ‘a’ will be equal to the ground voltage (VSS) level once condenser CD’s electrical charge has been discharged via SW.

   When VIN is higher than release voltage condenser CD will start to be charged. Delay time can be defined as the time from when this charge commences until the voltage at ‘a’ is more than the threshold voltage value.

(*) Threshold voltage value is the value the output block judges the signal by.

### A3. Electrical Discharge of the IC’s Internal Capacitor

In order to utilize delay time, it is necessary to fully discharge the condensor’s (CD) electrical charge during detect operations.
In terms of input, ‘High Level’ = 6V and ‘Low Level’ = 1V.
The required discharge time (T) therefore needs to be less than 300 μsec in order to fully utilize delay time. Please refer to the diagram below.